Review of Various Suitable PWM Methods for three Phase Multi-Level Inverters

Ankita Kumari[a*] and Nikhil Kumar Nigam [b**]
[a]*M. Tech*, Department of Electrical Engineering,*
Rajasthan College of Engineering for Women,
Jaipur, Rajasthan, India
[b]*Department of Electrical & Eletronics Engineering,*
Delhi Technical Campus, Greater Noida, UP, India
*Ankitalohan313@gmail.com, **n.nigam@delhitechnicalcampus.ac.in

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ABSTRACT

A multi-level inverter makes use of many DC voltage levels to produce the desired frequency alternating voltage at the output from a fixed DC supply whereas conventional two-level inverter uses only two level -VDC/2 and +VDC/2. For this reason, the Alternating voltage at the output has large harmonic distortion. Use of many voltage levels by the inverter for the production of output alternating voltage facilitates in reducing the harmonic contents present into the output voltage. Conventionally sinusoidal PWM method was in use but the method was not able to utilize the DC bus voltage efficiently. So other methods were presented and paper presents the literature the review of modified and improved PWM methods.

Keywords - SPWM, BCPWM, THIPWM, Multilevel Inverter, MLI, Harmonics

1. INTRODUCTION

In Recent times, the multilevel inverters have gained much attention of researchers because of high power quality output with low harmonic contents, less circuit complexity, and reduced switching losses. Two-level inverter converts single voltage level Vdc to two different voltage levels i.e. +VDC/2 and –VDC/2 for the load to produce an AC voltage. Though this technique of producing AC voltage from DC voltage is effective but it has some downsides as it produces harmonic distortions in the output voltage waveform. The concept of multilevel inverters is a kind of updated version of two-level inverter. Multilevel inverters produce smoother stepped output waveform in contrast to two-level inverter output. More than two voltage levels are used to produce the necessary output waveform. This also facilitates the use of power electronic devices with lower dv/dt rating. When the voltage level increases the harmonic distortions will reduce accordingly, but ultimately complication in the controller circuit and components also increases along with it. Most commonly there are three types of multilevel inverters are available, and these are 1. Diode Clamped multilevel inverters 2. Flying Capacitor multilevel inverters and 3. Cascaded H-bridge multilevel inverters (Congzhe Gaoet al., 2013; Qiang Songet al., 2013). The subsequent sections will direct the view on the selection of MLI among different MLI topologies with suitable PWM methods.

2. DIFFERENT TOPOLOGIES OF MULTI LEVEL INVERTER

Diode clamped inverters use clamping diodes to limit the potential stress on power electronic devices in the circuit. These were initially proposed in the year of 1981 and are also termed as neutral point clamped (NPC) converter.

A n level diode clamped inverter requires (2n – 2) switches, (n – 1) input voltage sources and (n – 1), (n – 2) diodes in order to work (Daniel Montesinos, et al., 2013; H. Zhanget al., 2000). The two prominent downsides of this type of inverter are higher number of clamping diodes are required with the increase in voltage level. The advantage of better efficiency and use of small capacitances make it a better choice over other topologies. This inverter finds major application in high voltage power drives and in power compensators (M. Hagiwara, et al., 2009).

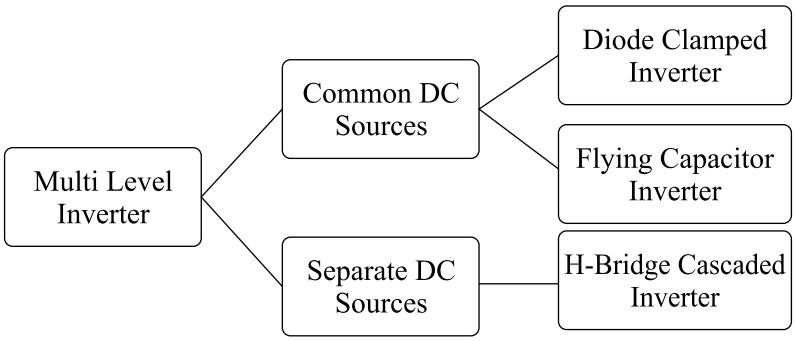

Figure 1 : Classification of Multi level Inverter

Flying capacitor inverters use capacitors to clamp the voltages. It consists of series connected clamped capacitors to reduce the voltage stress on the switching devices i.e. diodes for clamping to the DC bus are not needed in these multi-level inverters. The voltage between capacitors is available at the output terminals. In flying capacitors MLI switching states are same as are in the diode-clamped inverter. The use capacitors instead of diodes adds some drawbacks in the topology, which are, diodes have the ability to block the reverse flow of voltage but capacitors do not have such ability, Also the cost of capacitors is higher than the diodes. The number of switches also increases which lead higher switching losses (M. Hagiwara, et al., 2010; Xiaojie Shiet al., 2013).

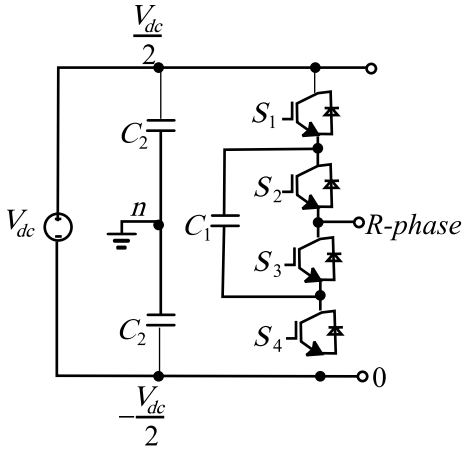

Figure 2a: Three level Flying Capacitor Inverter

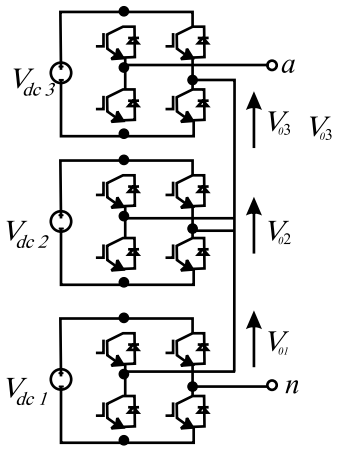

Figure 2b: H Bridge Cascaded Inverter

A n-level flying capacitor inverter will use (2n – 2) power switches and n number of capacitors. Figure:1a shows a three-level flying capacitor multilevel inverter. These are best used in Static VAR compensators for controlling the real and reactive power flow.

Cascaded H-Bridge MLI makes use of many series connected H-bridges to produce the sinusoidal voltage at the output. Each cell has one H-bridge and the output voltage generated is the algebraic sum of the voltages produced by each cell. If inverter has n-cells in a H-bridge multilevel inverter then number of output voltage levels will be 2n+1. This inverter is popular over other two inverters as this topology requires low rated power electronic switches as compared to the other two types of inverters (Bhuvaneswari, V. et al., 2015). The total harmonic distortion in the output voltage can be minimized by suitably selecting the switching angles of this H-Bridge inverter [(Omer, P. et al., 2014; S. De, et al., 2011).

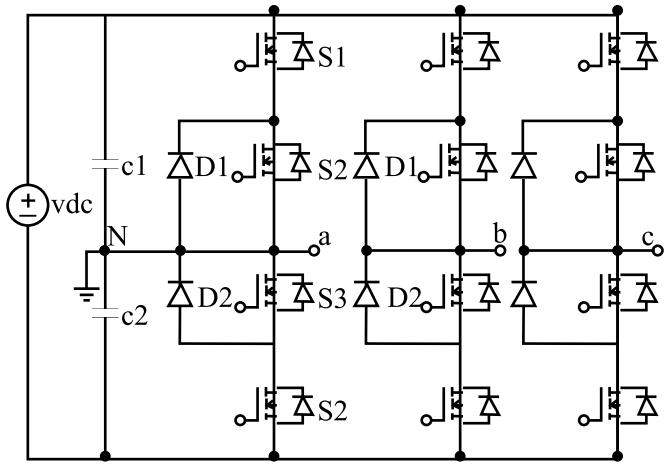

Figure 3c: Diode Clamped Multi-level Inverter

Figure 2b shows the topological structure of three level Cascaded H-Bridge Inverter, where each H-Bridge Cell consists of four switches. Different combinations of switch positions provide different voltages such as 0,+ VDC and -VDC. It does not need any capacitor or diode for clamping purposes. The output waveform has lower harmonic even without any filter circuit. At least three voltage levels will be required for a multilevel inverter and same can be achieved by a single H-Bridge unit in Cascaded H-Bridge MLI. Table 1 provides the Comparison of Multi Level Inverter Topologies illustrating the number of power electronic switches, clamping diodes and capacitors in detail.

Table 1: Comparison of Multi Level Inverter Topologies

S. No.		Diode Clamped	Flying Capacitor	Cascaded H-Bridge
1	Power Electronic Switches	2(n-1)	2(n-1)	2(n-1)
2	Clamping Diodes per phase	(n-1).(n-2)	0	0
3	DC Bus capacitors	(n-1)	(n-1)	(n-1)/2
4	Balancing capacitors per phase	0	(k-1)(k-2)/2	0
5	Voltage Unbalancing	Average	High	Very Small

In addition to the above-mentioned factors, the inverter efficiency and THD also depends on the type of PWM technique which is being used with the particular topology. So, selection of a suitable PWM technique is essential in multi-level inverter.

3. MULTILEVEL INVERTER MODULATION METHODS

The development of various multilevel inverter topologies posted the challenge to cover traditional modulation methods to the new multilevel inverter topologies. The Challenges were to accommodate the inherent complexity of having more power-electronics switches to regulate along with it to search the possibility to take benefit of the extra degrees of freedom provided by the additional switching states produced by these topologies (B. P. McGrath, et al., 2002; S. Rohner, et al., 2009). This led to the large number of different modulation procedures adapted or developed which were application and the inverter topology specific, each one having unique upsides and downsides. A classification of the most common modulation approaches for multilevel inverters is presented in Figure 2 (L. M. Tolbert, et al., 2000).

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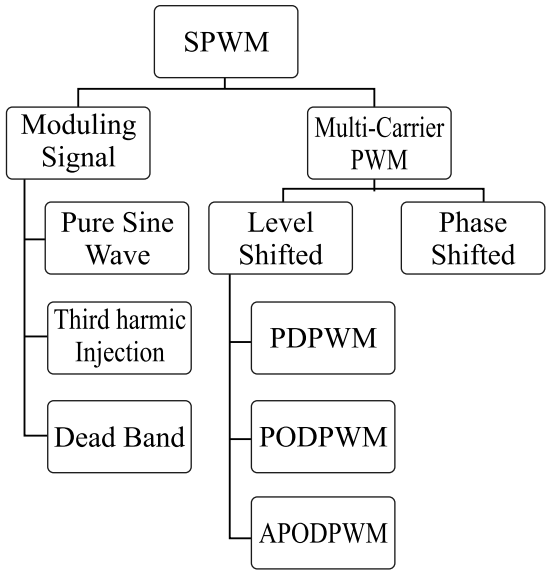

Figure 4 : Classification of SPWM Techniques

Based on the carrier signal frequency, switching frequency are classified into two types. One is high frequency range, which is above 3 KHz to 11 KHz and other one is low frequency range, which is closer to the fundamental frequency i.e. 500 Hertz. The reason to Shift on to the high carrier signal switching techniques, is to reduce the lower order harmonic contents, but it will cause high switching loss because of fast switching operations. To reduce the switching losses, low frequency switching may be preferred, but this will cause increased lower order harmonics in the output Voltage.

For very frequency switching, multi carrier modulation techniques were devised. The commonly used MCPWM techniques are PD, POD and APOD. In Phase Disposition technique all carrier waveforms are in phase, whereas in POD all +ve magnitude carrier waveforms are in phase and are 180° out of phase with -ve magnitude carrier signals and in APOD every carrier signal is 180°out of phase with its neighbouring carrier signal. Improving the output waveform is also related to the increase in the number

of output levels. Increased number of levels results in the output waveform which is closer to the fundamental frequency signal with less harmonic distortion. In a given simulation result nine level multilevel inverter haslesser THD level compared to 5 or 3 level multilevel inverter. Reducing the carrier switching frequency also reduces the THD level. When the inverter is switching at high frequency, the waveform becomes less distorted.

So, PWM method with higher switching frequency is the alternate to overcome the demerits associated with low switching (Leo Sekar G., et al., 2016; J. S. Reddy, et al. 2019).

4. RESULT

In this Harmonic analysis of SPWM, THIPWM and BCPWM controlled voltage source inverter the carrier signal frequency is varied from 1000 Hz to 3000 Hz.

Table-2 shows comparative THD_V and THD_I values of VSI with SPWM, THIPWM and BCPWM control approaches.

Minimum THD_V and THD_I for SPWM fed inverter are 65.98 % and 2.06 % respectively, are obtained at carrier frequency of 2000 Hertz.

Minimum THD_V and THD_I for THIPWM fed inverter are 53.89 % and 1.57 % respectively, are obtained at carrier frequencies of 2000 Hertz and 3000 Hertz respectively. Usually minimum current THD is consider as the best for selecting the appropriate carrier frequency for a circuit. It can be suggested to consider 3000 Hz as carrier frequency for THIPWM controlled inverters as THD_I is minimum.

Minimum THD_V and THD_I for BCPWM fed inverter are 51.35 % and 1.34 % respectively, are obtained at carrier frequencies of 2000 Hertz and 3000 Hertz respectively. It can be suggested to consider 3000 Hz as carrier frequency for BCPWM controlled inverters as THD_I is minimum.

Table -2 : The variation of THDV and THDI for SPWM, THIPWM and BCPWM controlled three-phase VSI (J. S. Reddy, et al. 2019)

Carrier Signal	**SPWM**		**THIPWM**		**BCPWM**	
Frequency (Hz)	THDV(%)	THDI(%)	THDV(%)	THDI(%)	THDV(%)	THDI(%)
1000	72.97	3.40	62.81	2.80	56.19	2.13
1500	71.55	2.39	67.80	2.03	57.60	2.00
2000	65.98	2.06	53.89	1.77	51.35	1.67
2500	87.69	2.30	76.70	1.64	67.03	1.54
3000	71.61	2.11	63.49	1.57	53.02	1.34
Fundamental Frequency for THD calculation = 50 Hz						

4. CONCLUSIONS

A 3 level three phase VSI case studies were studied with SPWM, THIPWM and BCPWM control strategies. Analysis study of various research papers of THDV and THDI is done at carrier frequencies from 1000Hz to 3000Hz. THDV and THDI Simulation results of SPWM, THIPWM and BCPWM are compared. From Table 2 it can be concluded that BCPWM provides best quality of output voltage and current when compared to SPWM and THIPWM controlled inverter i.e. both THDV and THDI is lesser in case of BCPWM. Although there is variation in THDV and THDI with variation in Carrier signal frequency and it is clear that THDI is well below 5% as specified by IEEE standards in all SPWM, THIPWM & BCPWM inverters considering 50 Hz as the fundamental frequency.

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