Analysis of Current Mirrors for Low Power

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Abstract

This paper deals with the development of low power current mirrors which uses level shifter technique. We also introduce a modified current mirror which is advancement in conventional current mirror. The modified current mirror gives twice bandwidth as compared to simple current mirror. T-SPICE simulations based on models for 1. 2 micron technology, validate the operation of the proposed current mirrors for current of 500uA with reduction in power level up to 65%.

Keywords - LS-Level Shifter, CM- Current Mirror

Introduction

A basic current mirror is formed by two MOS transistors (Allen and Holberg, 1987). The first MOS transistor M1 is coupled as a diode-connected device and it generates a bias voltage in response to an input current (Iref). The second MOS transistor M2 receives the bias voltage at a gate terminal and generates an output current (Iout) at its drain terminal which is proportional to the input current. If two transistors are perfectly matched then we get the same current on both transistors.

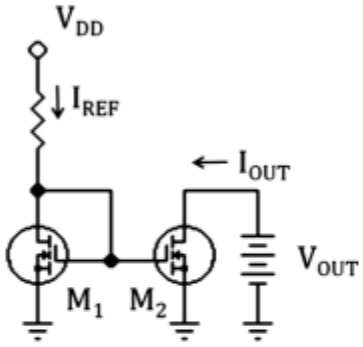

Figure 1: Simple current mirror

The current mirror shown work above a minimum voltage which is known as threshold voltage and they cannot work in sub threshold region.

But today with the improvement in technology the need of reducing power consumption in the circuits is increasing at an alarming rate. So, there is also a need of reducing power in the current mirror circuits also.

Many attempts have been made to reduce the power consumption in current mirror and one of the attempts is level shifter technique. With the help of level shifter technique, (Rajput and Jamuar, 2002; 2003) we can reduce the minimum voltage to a great extent and the current mirrors can be made to work in the sub threshold region (Rajput and Jamuar 2001). In this technique we introduce a PMOS transistor in between the two NMOS transistor of current mirror.

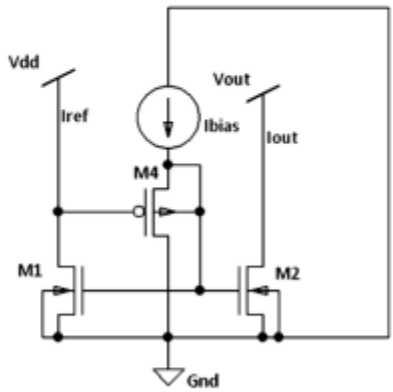

Figure 2: Level shifter current mirror

The minimum voltage required in this technique is Vgs1-Vgs4. Appropriate value of Ibias is selected to provide necessary current to the PMOS transistor. By this technique we have implemented all the current mirrors and found that there is reduction in power level up to 65%.

Modified Current Mirror

An improvement has been done in conventional current mirror to increase its bandwidth by a factor of 2 i.e. to make it twice (Gupta *et al.*, 2009). In simple current mirror a resistance of value 1/gm1 i.e. inverse of trans conductance is introduced between the gate and drain of the transistor which is in diode connected load configuration. The introduction of the resistance does not affect any small signal parameter but results in increase in bandwidth.

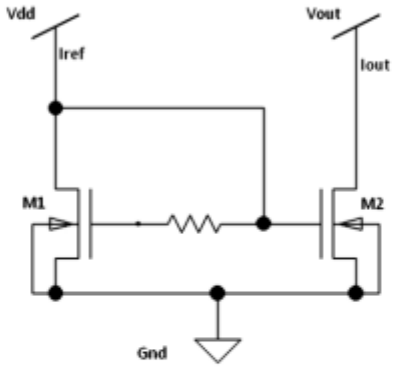

Figure 3: Modified current mirror

Bandwidth Calculation

To calculate bandwidth of the modified current a small signal model of the modified current mirror is made as shown in Fig. 4. In this model we have considered that only gate to source capacitance (cgs) exists and all other capacitances are negligible.

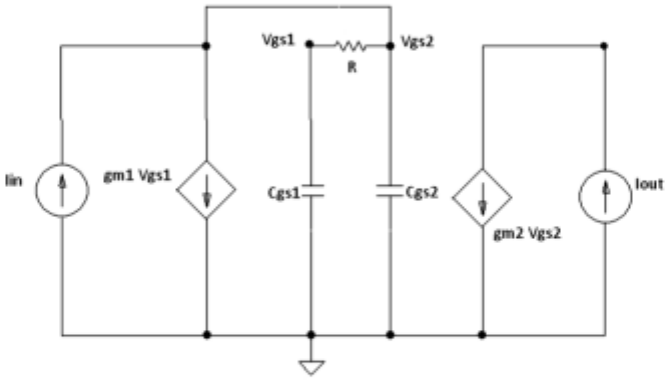

Figure 4: Small signal model of modified current mirror

Applying KCL at input side we get

$$Iin = gm_1 Vgs_1 + sVgs_2 cgs_2 + sVgs_1 cgs_1$$

Applying KCL in the resistance block we get

$$(Vgs_2 - Vgs_1)/R = sVgs_1 cgs_1$$

Solving these equations we get

$$Iin = Vgs_2(gm_1 + s\,cgs_1 + s\,cgs_2 + s^2R\,cgs_1cgs_2)/1 + sRcgs_1$$

Applying KCL at output side we get

$$Iout = gm_2 Vgs_2$$

And Finally we get

$$Iout/Iin = gm_2(1+sRcgs_1)/gm_1 + scgs_1 + scgs_2 + s^2Rcgs_1cgs_2$$

Now we have boundary conditions as

- $cgs_1 = cgs_2 = cgs$
- $R = 1/gm_1$

Applying these boundary conditions we get

$$Iout/Iin = (gm_2/gm_1)/(1 + s\,cgs/gm_1)$$

If we calculate 3db bandwidth for the above equation we will get it as follows

$$w_{3db} = gm_1/cgs$$

While for the simple current mirror with the same boundary conditions it was $gm_1/2cgs$. So we can see that the bandwidth has become twice.

Current Mirror Circuits with Level Shifter Technique

The conventional and level shifter current mirror circuits shown below are designed and evaluated in T-SPICE using 1.2 micron technology with the current of 500uA and W/L ratio of 2.5/1.2 and 21/1.2.

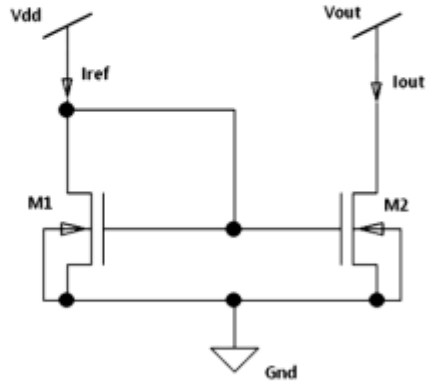

Figure 5: Simple current mirror

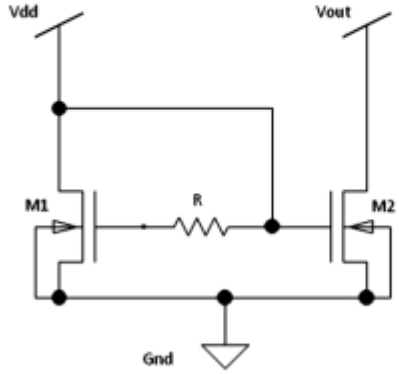

Figure 6: Modified current mirror

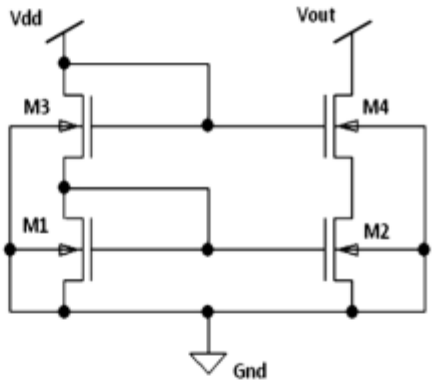

Figure 7: Cascade current mirror

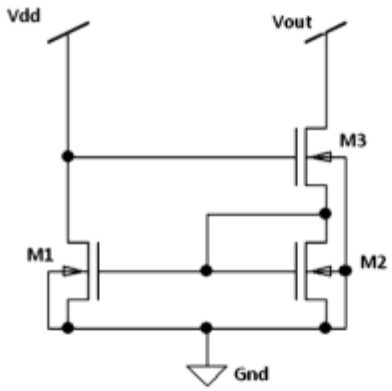

Figure 8: Wilson current mirror

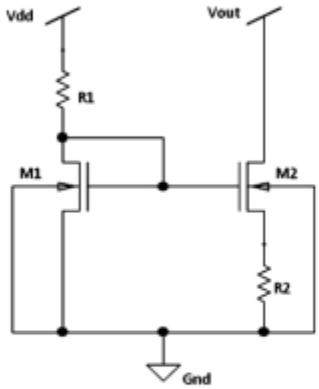

Figure 9: Widlar current mirror

Analysing the current mirrors shown above from Fig. (5-9) at different W/L ratio i.e. 21/1.2 and 2.5/1.2 with same current 500uA & channel length modulation parameter(λ) 0.001V-1 we get the following results :

Level shifter current mirrors

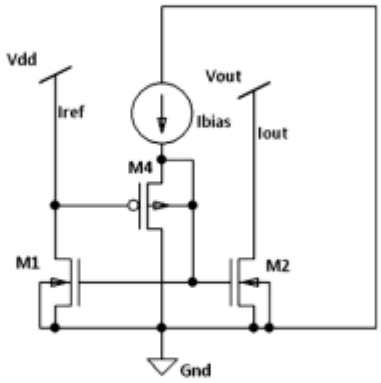

Figure10: LS-Simple current mirror

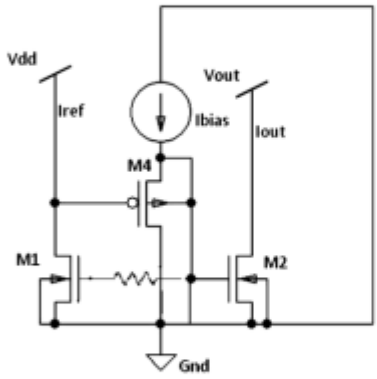

Figure11: LS-Modified current mirror

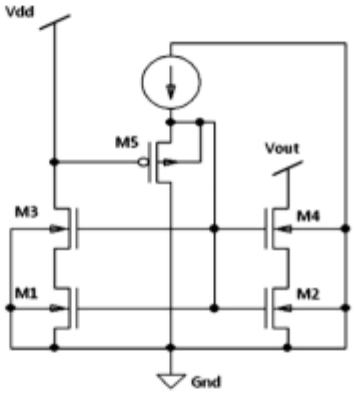

Figure 12: LS-Cascade current mirror

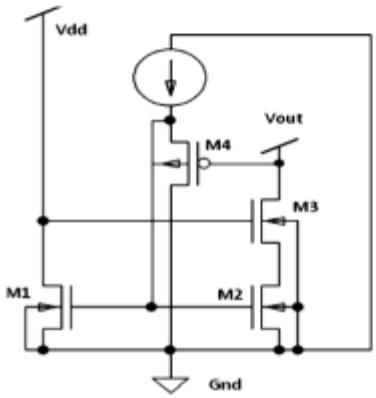

Figure 13: LS-Wilson current mirror

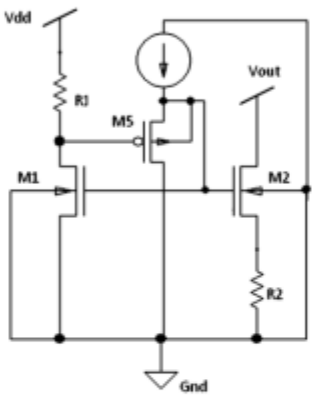

Figure 14: LS-Widlar current mirror

Now all these circuits are compared with the conventional current mirror circuits for the current of 500uA, W/L ratio 21/1.2 and channel length modulation parameter (λ) 0.04V-1 except the Wilson current mirror. At λ as 0.04 V-1 its W/L ratio has to be changed. The results are as follows:

Table 1: Comparison of different current mirrors having W/l=21/1.2

Properties	Simple CM	Modified CM	Cascode CM	Wilson CM	Widlar CM
Voltage(V)	1.419	1.419	2.838	2.838	2.92
gm(in e-03)	1.38	1.38	1.38	1.38	1.39
gds(in e-07)	4.99	4.99	4.99	4.99	5.00

Table 2: Comparison of different current mirrors having W/l=2.5/1.2

Properties	Simple CM	Modified CM	Cascode CM	Wilson CM	Widlar CM
Voltage(V)	2.785	2.785	5.57	5.57	5.29
gm(in e-04)	4.91	4.91	4.91	4.91	4.92
gds(in e-07)	4.99	4.99	4.99	4.99	4.99

By this comparison it was found that increase in W/L ratio results in decrease in input voltage and increase in trans-conductance (gm) but output conductance (gds) remains same. So W/L ratio has no effect on gds.

Table 3: Comparison of trans conductance (gm) with W/l ratio

W/L ratio	Tran conductance (gm)
21/1.2	1.38 e-03
2.5/1.2	4.91 e-04

So it can be seen that for 8.4 times increase in W/L ratio there is an increase of 2.8 times in Tran conductance (gm).

Table 4: Comparison of conventional V/S LS current mirror

Properties	Simple CM	Modified CM	Cascode CM	Wilson CM	Widlar CM
Power (mW)	.7	.7	1.4	1.4	2
LS Power (mW)	.354	.354	.5	.79	1.68
gm (in e -03)	1.46	1.46	1.46	1.46	1.46
LS gm (in e-03)	1.38	1.38	1.38(m4) / 0.584(m2)	1.45(m3) / 0.336 (m2)	1.43
gds (in e-05)	1.89	1.89	1.89	1.89	1.72
LS gds (in e-05)	3.81	3.81	3.8 (m4) / 139(m2)	1.9(m3) / 265(m2)	1.76

By the table IV we can see that there is reduction in power level from 16% to 65%. So the level shifter technique is successfully implemented in all the current mirrors.

Current Mirror using Level Shifter

Iin 0 2 1nA

vdd 1 0 dc 0.708v

vout 3 0 dc 0.708v

m1 1 2 0 0 mosn w=21u l=1.2u ad=7.5u pd=8.5u as=7.5u ps=8.5u

m2 3 2 0 0 mosn w=21u l=1.2u ad=7.5u pd=8.5u as=7.5u ps=8.5u

m4 0 1 2 2 mosp w=2.4u l=1.2u ad=7.5u pd=8.5u as=7.5u ps=8.5u

model mosn nmos vto=0.7 kp=110u Gamma=0.40 Lambda=0.04 Phi=0.7.

model mosp pmos vto=-0.7 kp=50u Gamma=0.57 Lambda=0.57 Phi=0.8.

tran .5n 100n.

print tran i(m1) i(m2).

power vout 0ns 100ns.

Power vdd 0ns 100ns

Power results

vdd from time 0 to 1e-007

Average power consumed -> 3.545195e-004 watts

Max power 3.545195e-004 at time 0

Min power 3.545195e-004 at time 0

LS-Modified Current Mirror

Iin 0 2 1nA

vdd 1 0 dc .707v

vout 3 0 dc .707v

r 4 2 147

m1 1 4 0 0 mosn w=21u l=1.2u ad=7.5u pd=8.5u as=7.5u ps=8.5u

m2 3 2 0 0 mosn w=21u l=1.2u ad=7.5u pd=8.5u as=7.5u ps=8.5u

m4 0 1 2 2 mosp w=2.4u l=1.2u ad=7.5u pd=8.5u as=7.5u ps=8.5u

model mosn nmos vto=0.7 kp=110u Gamma=0.40 Lambda=0.04 Phi=0.7.

model mosp pmos vto=-0.7 kp=50u Gamma=0.57 Lambda=0.57 Phi=0.8.

tran .5n 100n.

op.

(print tran i(m1) i(m2.

power vout 0ns 100ns.

power vdd 0ns 100ns.

probe.

End

Power results

vdd from time 0 to 1e-007

Average power consumed -> 3.540898e-004 watts

Max power 3.540898e-004 at time 0

Min power 3.540898e-004 at time 0

LS-Cascode Current Mirror

Iin 0 5 1nA

vdd 1 0 dc 1.007v

vout 2 0 dc 1.007v

m1 4 5 0 0 nmos w=21u l=1.2u AD=7.5p PD=8.5u AS=7.5p PS=8.5u

m2 3 5 0 0 nmos w=21u l=1.2u AD=7.5p PD=8.5u AS=7.5p PS=8.5u

m3 1 5 4 0 nmos w=21u l=1.2u AD=7.5p PD=8.5u AS=7.5p PS=8.5u

m4 2 5 3 0 nmos w=21u l=1.2u AD=7.5p PD=8.5u AS=7.5p PS=8.5u

m5 0 1 5 5 mosp w=2.4u l=1.2u ad=7.5u pd=8.5u as=7.5u ps=8.5u

model nmos nmos vto=0.7v kp=110u gamma =0.4 lambda =0.04 phi=0.7.

model mosp pmos vto=-0.7 kp=50u Gamma=0.57 Lambda=0.57 Phi=0.8.

tran .5n 100n.

OP.

(print tran i(m1) i(m2) i(m3) i(m4.

power vdd 0ns 100ns.

power vout 0ns 100ns.

PROBE.

end

Power results

vdd from time 0 to 1e-007

Average power consumed -> 5.040232e-004 watts

Max power 5.040232e-004 at time 0

Min power 5.040232e-004 at time 0

Conclusion

After implementing all the conventional and level shifter current mirrors using 1.2 micron technology it was observed that the huge power reduction is obtained in the current mirrors. This power reduction is basically due to operation of current mirror in sub threshold region. The reduction in power level is from 16% to 65%. The minimum power reduction is achieved in widlar current mirror while most power reduction is achieved in cascade current mirror. The proposed modified current mirror is also showing approx. 50% power reduction while providing twice bandwidth as compared to simple current mirror. The LS-cascade current mirror can also be used in case of conventional current mirrors as it shows maximum power reduction and the output resistance is also very high.

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