Role of Gate Materials in Performance Enhancement of Junctionless Vertical Double Gate MOSFET

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Abstract

In this paper, we propose a novel design analysis for a Junctionless Double Gate Vertical MOSFET (JLVMOS) with metal gate electrode, for which the simulations have been performed using TCAD (ATLAS), the simulated results exhibits significant improvements in comparison to conventional JLVMOS device with a polysilicon gate electrode at 45nm gate length. In place of polysilicon gate we have used metal gate and observed that metal gate electrode in JLVMOS shows ON current is 0.981 mA, for a gate voltage of 1V and an average subthreshold swing and DIBL (Drain Induced Barrier Lowering) are 67.4mV per decade and 61.59mV/V respectively. This significant improvement in ON current can be exploited for various high-performance circuit applications.

Keywords- Junctionless Vertical Double Gate MOSFET (JLVMOS), Leakage current (IOFF), Subthreshold Swing, TCAD Tool.

Introduction

The scaling of CMOS technology in to nano meter regime requires alternative device structures in overcoming a number of short channel effects and leakage current. The formation of PN junction between the source/drain and channel become a fabrication challenge beyond 32 nm CMOS technology. A lot of novel double gate MOSFET structures have been proposed and widely investigated by number of researchers (Ismail, 2009). The junctionless double gate vertical MOSFET has been proposed recently. The junctionless VMOS is free from variety of challenges related to formation of source –drain junction with substrate and hence present a very suitable candidate for future deca nanometer MOSFET applications. In junctionless VMOS, the doping level in the semiconductor source, drain and substrate is identical (n-type: N^+ - N^+ - N^+ and p-type: P^+ - P^+ - P^+) and there is no formation of P-N junction between the source –drain and channel (Xin and Yinglin, 2011). Gate is highly doped with p-type impurity (boron) to maintain the threshold voltage.

The advantages of vertical MOSFET is that it does not require next generation or advanced lithography to achieve a small memory area or a short channel length because it's defined by the sub lithography of layer

thickness and etching (Mistry, 2007). The requirement of memory and logic application is different; on the one hand, memory cell area should be small for higher density so It can be achieved by using vertical MOSFET with foot print but long channel length to reduce the OFF state current of circuit but the channel length for high performance logic should be short as much as possible for high ON state current.

In junctionless VMOS, the controlling capability of gate over the channel region, resulting in reduced short-channel effects (SCEs) (Chih-Husan *et al*., 2010). The fabrication process of junctionless MOSFET is highly simplified, in comparison to conventional CMOS technology (Rahul *et al*., 2012). Since there are no doping concentration gradients required during the time of fabrication in the device, it also saves a lot of thermal budget (Rahul *et al*., 2012). The vertical channel of a VMOS is defined by gate spacer due to which the fabrication cost can be decreased drastically (Chun-jen, 2009). The metal gate electrode in junctionless double gate vertical MOSFET has not been investigated Up to now.

In this paper, the metal gate with a tunable work function ranging from 5.10eV to 5.20eV has been investigated in JLVMOS for performance enhancement by using our two dimensional ATLAS simulator.

Device Structure and Simulation

The TCAD Tool package (DEVEDIT) is used to design the device structures and perform the relevant device simulations using ALTAS 2D simulator. The structure of JLVMOS with the double gate region (in contact), drain and source electrode, channel length (L_g), oxide thickness (T_{ox}), body thickness (T_{si}) or channel and the respective dimensions of the device are explicitly shown in Figure 1. The carrier depletion effect in the MOSFET due to the polysilicon gate electrode is also called as the poly depletion effect. It occurs when an applied electric field sweeps away carriers so as to create a region in the doped polysilicon where the non-mobile dopant atom becomes ionized. In p-doped polysilicon the depletion layer includes ionized non- mobile acceptor sites. This poly depletion effect reduces the strength of the expected electric field at the surface of the semiconductor when a voltage is applied to the gate electrode. The reduced electric field strength degrades the performance of the device (Wen-Chin, 1999).

Metal gate electrode removes the carrier depletion effect observed in polysilicon gate electrode. It improves the device performance, at the same time, by maintaining the work function (ΦM) equal or at least near to the value of polysilicon gates. The threshold voltage of JLVMOS is depends on the work function (ΦMS) difference between the semiconductor and the material using at gate electrode. The metal gate electrode with work function near to 5.27 eV can replace the p- doped polysilicon typically found in N-type junctionless MOSFET (Dennard, 1974).

We assumed high channel doping concentration ($1\times10e^{-19}cm^{-3}$) for less V_t variations. Silicon film thickness and oxide (SiO2) thickness are 10 nm and 2nm, respectively. We assumed N-channel device and simulated the device for different work function of metal gates of junctionless VMOS. A good match of work function can be obtained by using nickel (Ni) and gold (Au) metal for gate electrodes of JLVMOS. The work function found in p-doped polysilicon approximately 5.27 eV. We assumed nickel metal for metal gates because it provides wide range of work function. Metal gate technology may potentially replace conventional polysilicon gate technology for juctionless devices for better performance.

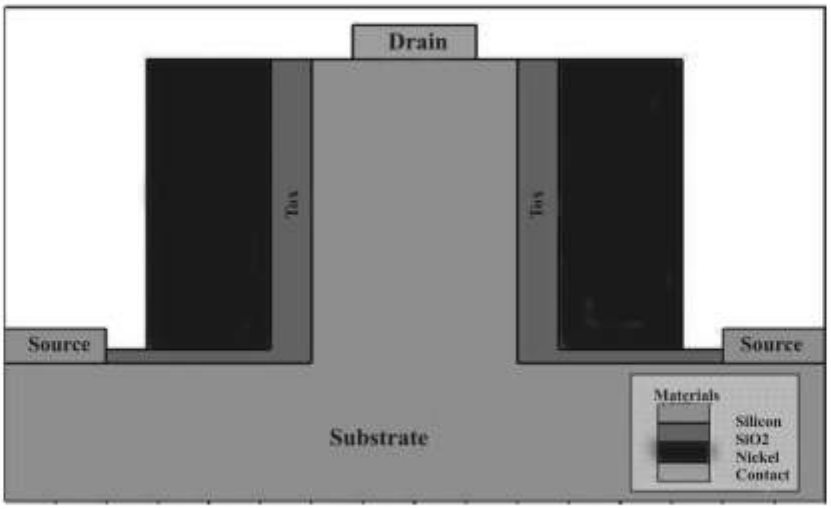

Figure 1: 2D Structure of Junctionless Vertical Double Gate MOSFET.

Results and Discussion

The I_d-V_{gs} characteristics of junctionless vertical double gate MOSFET is shown in Figure 2 and I_d-V_{ds} characteristics are shown in Figure 3; drain current of JLVMOS with work function Φm of 5.10 eV is 0.981 mA which is high comparison to the JLVMOS with polysilicon gate. The I_d-V_{ds} characteristics of JLVMOS has been obtained at gate voltage of 1.0 V and found that when we decreases the work function of gate electrode the drain current of JLVMOS start to increase because the channel surface below the gate electrode start accumulating earlier and produce large drain current without adding any extra doping in to the substrate.

The JLVMOS structures with high work function Φ_m = 5.20eV have lower DIBL (drain induced barrier lowering), subthreshold swing, low leakage current and higher threshold voltage as compared to devices having gate electrode with work function Φ_m = 5.10 but lower drain current shown in Table 1. The JLVMOS having metal gate electrode with work function Φ_m 5.10 eV has higher value of Idmax (maximum drain current) compared to metal gate device with work function Φ_m 5.20eV, 5.15eV and polysilicon gate electrode, but it has higher leakage current and DIBL. So by providing the different work function of metal gates to JLVMOS device we can set the appropriate threshold voltage. So we are able to increase the drain current according to our requirements without adding any extra doping in to the channel because drain current is affected by work function of metal gate electrode. Advantages of metal gate over polysilicon gate are there is virtually no depletion, no boron penetration, and sheet resistance is very low.

Table1: Comparison table of JLVMOS with metal gate electrodes and polysilicon gate electrode.

Device	Idmax (A/um)	S.Swing (mV/decade)	DIBL (mV/V)
JLVMOS (Poly-Si gate)	7.2×10^{-4}	63.74	44.29
JLVMOS (WF=5.20 eV)	8.05×10^{-4}	64.94	52.3
JLVMOS (WF=5.15 eV)	8.92×10^{-4}	65.95	58.7
JLVMOS (WF=5.10 eV)	9.81×10^{-4}	67.10	61.4

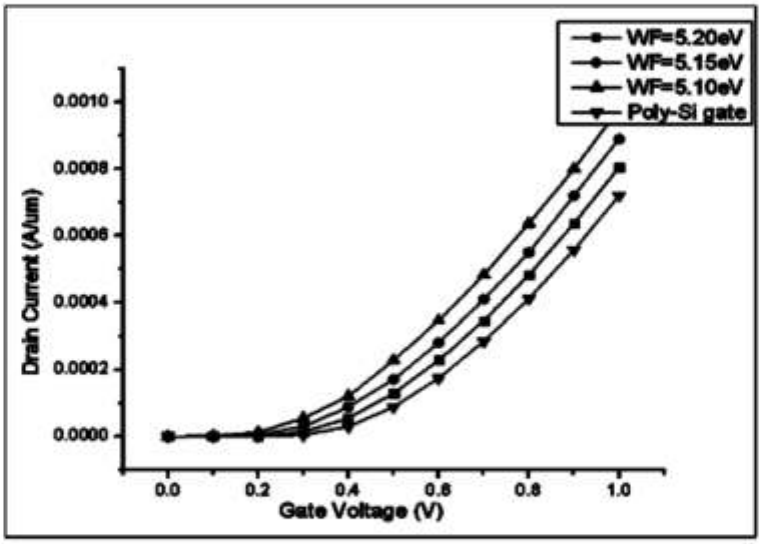

Figure 1: I_d-V_{gs} Characteristics of JLVMOS at 45nm technology.

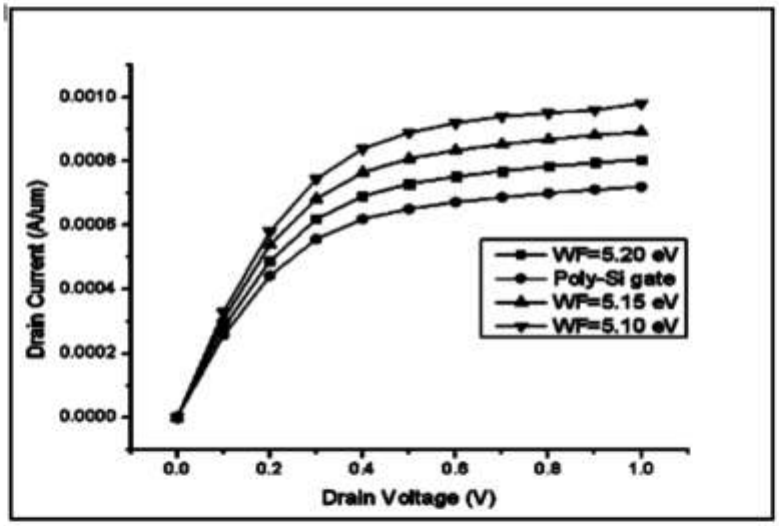

Figure 2: I_d-V_{ds} Characteristics of JLVMOS at different gate voltage of 45nm technology.

Conclusion

The work function engineering is the concepts by which we can set the appropriate threshold voltage of JLVMOS device that provide better device performance compared to the channel doping. The drain current of device can be increased by using metal gate electrode with low work function in comparison to polysilicon gate electrode because channel is already highly doped if we will add any extra doping in to the channel it will degrade carrier mobility in high temperature environment. It also allows a thinner effective dielectric thickness without affecting device performance. The metal gate electrode in JLVMOS with work function 5.10eV has produced highest drain current which is 36% more than the polysilicon gate electrode in same device and the DIBL effect, S. Swing and leakage current are still in the acceptable range.

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